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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,573	08/09/2001	Herbert Palm	P2000,0167 US	6959

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,573	Applicant(s) PALM ET AL.
	Examiner Thomas L Dickey	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *33-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☒ Claim(s) *30-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/900,654* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II, claims 1-32 in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

2. The oath/declaration filed on 24 September 2002 is acceptable.

Drawings

3. The drawings are objected to by the PTO Draftsperson for the reasons noted on the attached Notice of Draftsperson's Patent Drawing Review, form PTO-948.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/900,654, filed on 6 July 2001.

Information Disclosure Statement

5. The Information Disclosure Statements filed on 9 August 2001, 30 April 2002, and 16 July 2002 have been considered.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1,7,9-13,27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by BATE (4,360,900).

With respect to claims 1,7 and 9-13, Bate discloses a memory cell comprising: a semiconductor component having semiconductor material 20 and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer; a memory transistor including a source region 11-12 and a drain region 14-15 that are formed in said semiconductor material 20, said memory transistor including a gate electrode 13 located on said top side and located between said source region 11-12 and said drain region 14-15; a dielectric material 23-24-25 separating said gate electrode 13 from said semiconductor material 20; and a layer sequence including boundary layers and a memory layer located between said

boundary layers, said layer sequence located at least between said source region 11-12 and said gate electrode 13 and wherein at least one of said boundary layers includes Si_3N_4, which is a material that is selected from the group consisting of a nitride and an oxynitride, and wherein said memory layer is any of titanium oxide, tantalum oxide, or hafnium oxide, and thus is a material that is selected from any of the groups consisting of: undoped silicon, tantalum oxide, tantalate, hafnium silicate, hafnium oxide, titanium oxide, titanate, zirconium oxide, lanthanum oxide and aluminum oxide; tantalum oxide and tantalate; hafnium silicate and hafnium oxide; titanium oxide and titanate, or hafnium oxide, lanthanum oxide, and aluminum oxide. Note figure 3a and column 5 lines 27-30 of Bate.

With respect to claims 27 and 28, Bate discloses a memory cell configuration, comprising: a semiconductor component having semiconductor material 20 and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer; a plurality of memory cells that each include: a memory transistor including a source region 11-12 and a drain region 14-15 that are formed in said semiconductor material 20, said memory transistor including a gate electrode 13 located on said top side and located between said source region 11-12 and said drain region 14-15; a dielectric material 23-24-25 separating said gate electrode 13 from said semiconductor material 20; and a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region 11-12 and said gate electrode 13

and at least between said drain region 14-15 and said gate electrode 13; and a plurality of conductor tracks 26 defining word lines 16, said gate electrode 13 of each one of said plurality of said memory cells electrically conductively connected to one of said plurality of said conductor tracks 26; said source region 11-12 of one of said plurality of said memory cells defining said drain region 14-15 of an adjacent one of said plurality of said memory cells and said drain region 14-15 of said one of said plurality of said memory cells defining said source region 11-12 of another adjacent one of said plurality of said memory cells, wherein: said top side of said semiconductor material 20 defines a top surface; and said layer sequence is applied completely over said top surface of said semiconductor material 20 that is between said semiconductor material 20 and said gate electrode 13 of each one of said plurality of said memory cells and that is between said semiconductor material 20 and said plurality of said conductor tracks 26. Note figures 3a and 6 of Bate.

B. Claims 1-6,8-10,12-19,21-23,25, and 26 are rejected under 35 U.S.C. 102(a) as being anticipated by **HOFMANN** et al. (6,191,459).

Hofmann et al. discloses a memory cell comprising: a semiconductor component having semiconductor material 2 and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer; a memory transistor including a source region 10a and a drain region 10b that are formed in said semiconductor material 2, said memory transistor including a gate electrode 18 located on said top side and located between said source region 10a and

said drain region 10b; a dielectric material 17 separating said gate electrode 18 from said semiconductor material 2; the dielectric material 17 having a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region 10a and said gate electrode 18 and at least between said drain region 10b and said gate electrode 18, wherein said semiconductor material 2 has a trench formed therein and said gate electrode 18 is located in said trench. Note figure 8 of Hofmann et al.

With respect to claims 2,5,6,15,18, and 19, Hofmann et al. further discloses that one of said boundary layers faces said semiconductor material 2 and at least said boundary layer that faces said semiconductor material 2 is made of SiO_2, a material with a relative dielectric constant of at least 3.9 that is selected from the group consisting of an oxide and a silicate and has a barrier level of at least 2 eV is present between said semiconductor material 2 and said memory layer. Note column 2 line 57 of Hofmann et al. Applicants already admit that SiO_2 has a relative dielectric constant of at least 3.9, is selected from the group consisting of an oxide and a silicate, and has a barrier level of at least 2 eV. Note application, page 7 line 7, and page 6 line 21.

With respect to claims 3,4,8,16,17, and 21, Hofmann et al. further discloses that at least one of said boundary layers faces said semiconductor material 2 and at least said boundary layer that faces said semiconductor material 2 includes Ta_2O_5, a material that is selected from the group consisting of Al_2O_3 and Ta_2O_5 which has a relative dielectric constant of at least 20, and therefore a relative dielectric constant of at least 7.8. Note

particularly column 7 line 41 of Hofmann et al. Chang 6,001,742 supplies the proof that Ta_2O_5 has a relative dielectric constant of at least 20. Note column 3 line 24 of Chang.

With respect to claims 9,10,12,13,22,23,25, and 26, Hofmann et al. further discloses that said memory layer may include any of the following materials: tantalum oxide, aluminum, or titanium oxide. One or more of these materials meets one or more of claims 9,10,12,13,22,23,25, and 26, as required. Note column 2 line 62 of Hofmann et al.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over BATE (4,360,900) in view of HOFMANN et al. (6,191,459).

Bate discloses all the limitations of claim 29 except said semiconductor material has a plurality of trenches formed therein and said plurality of said trenches define walls; said gate electrode of at least one of said plurality of said memory cells is located in one of said plurality of said trenches; said memory layer is interrupted between a structure selected from the group consisting of said walls of one of said trenches and adjacent ones of said trenches.

However, Hofmann et al. discloses a memory cell configuration with a plurality of said memory cells, semiconductor material 2 having a plurality of trenches formed therein and said plurality of said trenches define walls; gate electrodes 18 in said trenches wherein said gate electrode 17 of at least one of said plurality of said memory cells is located in one of said plurality of said trenches; and said memory layer is interrupted between a structure selected from the group consisting of said walls of one of said trenches and adjacent ones of said trenches.

Therefore, it would have been obvious to a person having skill in the art to modify Bate's memory cell configuration with the a plurality of wall-defining trenches formed in the semiconductor material and a plurality of a trenches define walls; a gate electrode of at least one of a plurality of a memory cells is located in one of the plurality of trenches; where the memory layer (parts 23-24-25 in Bate, part 17 in Hofmann et al.; note that the memory layer is interrupted in both Bate and Hofmann et al., except there are no walls or trenches in Bate) is interrupted between the walls of the trenches, such as taught by Hofmann et al. in order to provide a vertical channel to thus provide a memory cell configuration where the channel length depends on the depth of the trenches rather than the distance between source and drain, allowing the memory cell configuration to scale down in size without short channel effect.

B. Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over HOFMANN et al. (6,191,459) in view of BATE (4,360,900).

Hofmann et al. discloses a memory cell comprising: a semiconductor component having semiconductor material 2 and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer; a memory transistor including a source region 10a and a drain region 10b that are formed in said semiconductor material 2, said memory transistor including a gate electrode 18 located on said top side and located between said source region 10a and said drain region 10b; a dielectric material 17 separating said gate electrode 18 from said semiconductor material 2; and a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region 10a and said gate electrode 18 and at least between said drain region 10b and said gate electrode 18, wherein said semiconductor material 2 has a trench formed therein and said gate electrode 18 is located in said trench. Note figure 8 of Hofmann et al.

Hofmann et al. does not disclose that at least one of said boundary layers includes a material that is selected from the group consisting of a nitride and an oxynitride, instead Hofmann et al. uses silicon oxide. Also, Hofmann et al. does not disclose that said memory layer is a material that is selected from the group consisting of hafnium silicate and hafnium oxide, instead Hofmann et al. uses, amongst other materials (the choice of material for the memory layer being non-critical), titanium oxide. However, Bate teaches that silicon nitride is interchangeable with silicon oxide, and hafnium oxide is interchangeable with titanium oxide, in a memory cell having a semiconductor material

20 and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer; a memory transistor including a source region 11-12 and a drain region 14-15 that are formed in said semiconductor material 20, said memory transistor including a gate electrode 13 located on said top side and located between said source region 11-12 and said drain region 14-15; a dielectric material 23-24-25 separating said gate electrode 13 from said semiconductor material 20; and a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region 11-12 and said gate electrode 13. Note figure 3a and column 5 lines 27-30 of Bate.

Therefore, it would have been obvious to a person having skill in the art to replace the silicon oxide boundary layer and titanium oxide memory layer of Hofmann et al.'s memory cell with the silicon nitride boundary layer and hafnium oxide memory layer such as taught by Bate. One skilled in the art would not do this in the sure expectation of gain; rather, following the teachings of Bate, one skilled in the art would understand that these substitutions might prove fruitful.

Allowable Subject Matter

8. Claims 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
04/2003